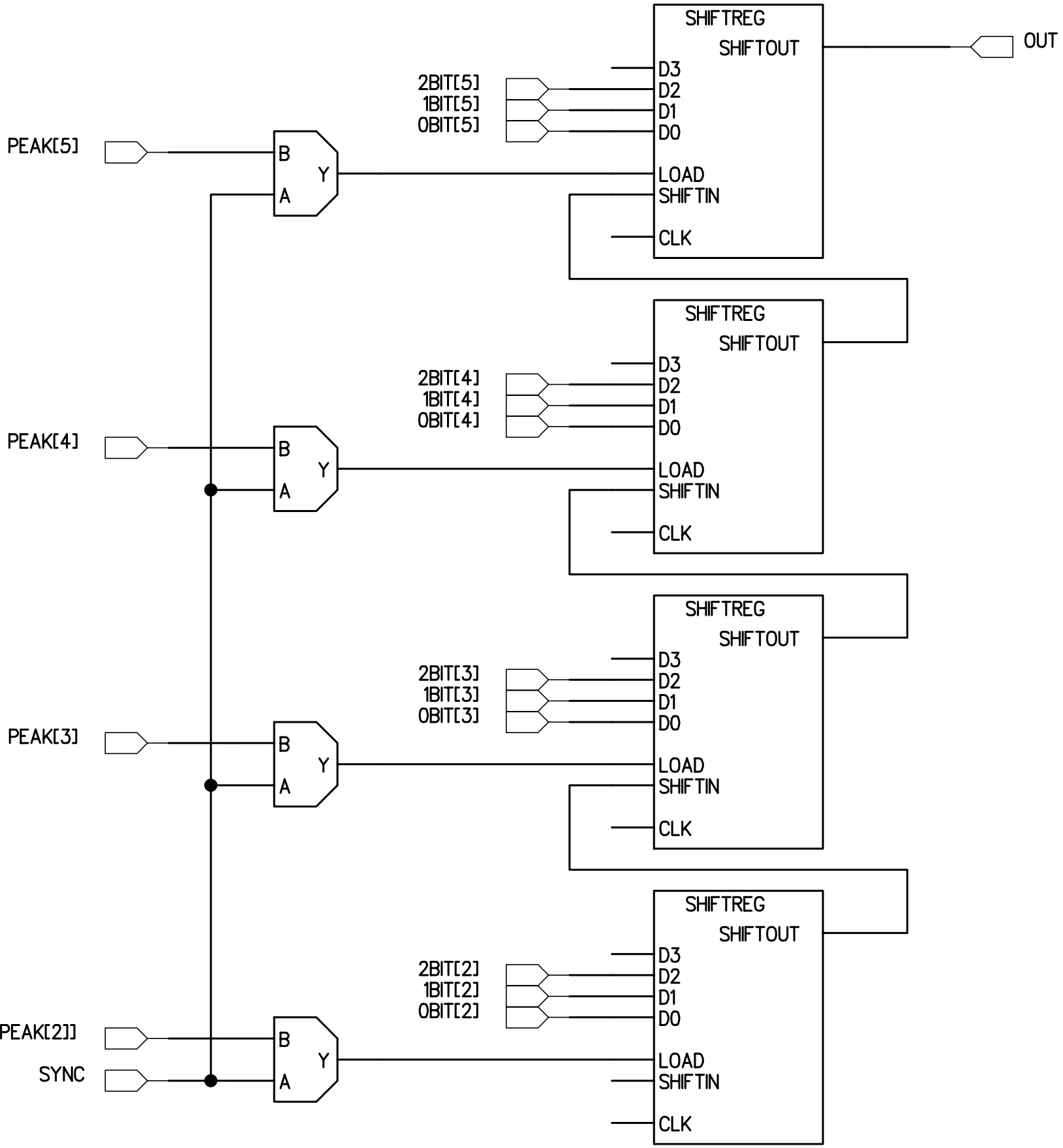
DATA


SHIFTREG
SHIFTOUT
D3
D2
D1
D0
LOAD
SHIFTIN
CLK
OUT
2BIT[5]
1BIT[5]
0BIT[5]
PEAK[5]
B
A
Y
2BIT[4]
1BIT[4]
0BIT[4]
PEAK[4]
2BIT[3]
1BIT[3]
0BIT[3]
PEAK[3]
2BIT[2]
1BIT[2]
0BIT[2]
PEAK[2]]
SYNC